PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2000-221926
(43)Date of publication of application : 11.08.2000

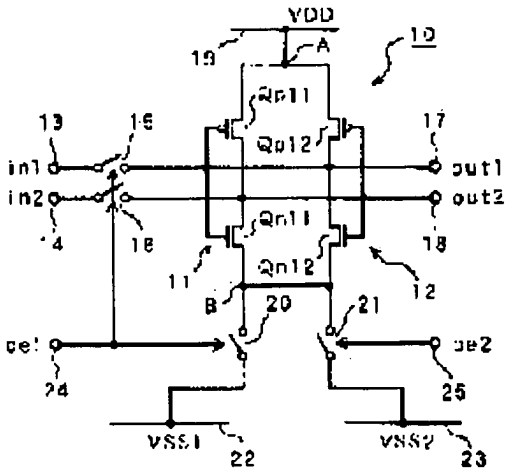
(51)Int.Cl. G09G 3/20
G02F 1/133
G09G 3/36
H03K 3/356

(21)Application number : 11-023384
(22)Date of filing : 01.02.1999

(71)Applicant : SONY CORP
(72)Inventor : NAKAJIMA YOSHIHARU
MAEKAWA TOSHIICHI

(54) LATCH CIRCUIT AND LIQUID CRYSTAL DISPLAY DEVICE MOUNTING THE SAME

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a latch circuit capable of suppressing a current flowing in a power supply, and capable of reducing the area, and a liquid crystal display device mounting the latch circuit.
SOLUTION: In this latch circuit having a CMOS latch cell 10 as a basic configuration and a level shift function, two switches 20, 21 for selecting a VSS1 power supply and a VSS2 power supply are installed on the negative power supply side of the CMOS latch cell 10, and switching control of the switches 20, 21 are executed corresponding to each period of a latch operation and an output operation of the CMOS latch cell 10, and the circuit is operated by the VSS1 power supply during the period of the latch operation and operated by the VSS2 power supply during the period of the output operation.



DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]About the liquid crystal display which carries latch circuitry and this, this invention makes especially a CMOS latch cell basic constitution, and relates to what is called a drive circuit integral-type liquid crystal display that carries latch circuitry with a level shift function, and this latch circuitry as one of the component circuits of a scanning system.
[0002]
[Description of the Prior Art]The conventional example 1 of latch circuitry with the level shift function which comprises CMOS is shown in drawing 10. The 1st and 2nd switch 101,102 that the latch circuitry concerning this conventional example 1 answers a latch pulse in the 1st and 2nd input signal in1 and in2, and is incorporated, It has the composition of having CMOS latch cell 103 which latches each signal incorporated by these switches 101,102, and the level shift circuit 104 which shifts the level of the latch data of this CMOS latch cell 103.
[0003]Here CMOS latch cell 103 The power source line 105 of the positive supply voltage VDD, and the negative supply side voltage. (For example, grand level) It consists of two CMOS inverters 107,108 connected in parallel between the power source lines 106 of VSS1, It is the circuitry to which the input edge of one CMOS inverter 107 and the outgoing end of CMOS inverter 108 of another side were connected to, and the input edge of CMOS inverter 108 of another side and the outgoing end of one MOS inverter 107 were connected.
[0004]Again The level shift circuit 104 is connected between the power source line 105 and the power source line 109 of power-supply-voltage (negative supply voltage) VSS2 lower than power-supply-voltage VSS1, The level shift of the low side of the data latched by CMOS latch cell 103 is carried out to power-supply-voltage VSS2 from power-supply-voltage VSS1.
[0005]In the latch circuitry concerning the conventional example 1 of the above-mentioned composition, the signal of the low-voltage amplitude of VDD-VSS1 shall be inputted as in1, and the inversion signal of signal in1 shall be inputted as in2. Signal in1 of this low-voltage amplitude and in2 are latched to CMOS latch cell 103, when one [a latch pulse is answered and / the switch 101,102], After that, a level shift is carried out to the signal of the amplitude of VDD-VSS2 (VSS2<VSS1) by the level shift circuit 104, and it is drawn as output signal out1 and out2.
[0006]The conventional example 2 of latch circuitry with a level shift function is shown in drawing 11. The 1st and 2nd switch 201,202 that the latch circuitry concerning this conventional example 2 answers a latch pulse in the 1st and 2nd input signal in1 and in2, and is incorporated, It has the composition of having CMOS latch cell 203 which latches each signal incorporated by these switches 201,202.
[0007]CMOS latch cell 203 consists of two CMOS inverters 206,207 connected in parallel between the power source line 204 and the power source line 205 of power-supply-voltage VSS2 lower than power-supply-voltage VSS1 here, It is the circuitry to which the input edge of one CMOS inverter 206 and the outgoing end of CMOS inverter 207 of another side were connected to, and the input edge of CMOS inverter 207 of another side and the outgoing end of one MOS inverter 206 were connected.

[0008]In the latch circuitry concerning the conventional example 2 of the above-mentioned composition, the signal of the low-voltage amplitude of VDD-VSS1 shall be inputted as in1, and the inversion signal of signal in1 shall be inputted as in2. When one [signal in1 of this low-voltage amplitude and in2 answer a latch pulse and / the switch 101,102], it is latched to CMOS latch cell 103 as a signal of the amplitude of VDD-VSS2, and the signal of this amplitude is drawn as output signal out1 and out2 as it is.
[0009]
[Problem(s) to be Solved by the Invention]However, in the latch circuitry concerning the conventional example 1 mentioned above, since it is necessary to allot the level shift circuit 104 to the latter part of CMOS latch cell 103 and the element number which constitutes this latch circuitry increases, there is a problem that small-area-izing is difficult. On the other hand, if it is in the latch circuitry concerning the conventional example 2, While only the part which does not need to provide a level shift circuit separately compared with the latch circuitry concerning the conventional example 1 is realizable with a small element number, in order to have to rewrite the latch for the signals of high-tension amplitude compulsorily by the signal of low-voltage amplitude, There is a problem that the size of the signal buffer of the preceding paragraph becomes large, and small area-ization becomes difficult too.
[0010]By the way, on the glass substrate (liquid crystal panel) in which poly-Si TFT (thin filmtransistor; thin film transistor) has been arranged as a switching element of each pixel at two-dimensional matrix form, In the drive circuit integral-type liquid crystal display which a picture element part and really forms a digital interface drive circuit by poly-Si TFT, on the occasion of the creation, when small area-ization of the above-mentioned latch circuitry attains narrow-ization of the adjacent spaces (frame) of the picture element part which forms a drive circuit, it serves as an important point.
[0011]Namely, the latch circuitry mentioned above in the drive circuit integral-type liquid crystal display, Since only the number of the dot number x numbers of bits indispensable as latch circuitry provided corresponding to each column line / each bit and horizontal as this latch circuitry is needed, it leads as a result that-izing of the latch circuitry cannot be carried out [small area] to the problem that the width of the frame of a liquid crystal panel spreads.
[0012]In the drive circuit integral-type liquid crystal display which carries latch circuitry with the level shift function mentioned above, there is a case where he would like to make small the current which flows into the 2nd power supply (the above-mentioned example VSS2 power supply) as much as possible. For example, it is a case where it is created by TFT, and the above-mentioned latch circuitry tends to be carried as one of the component circuits of a level drive system, and it is going to create the 2nd power generation circuit by TFT simultaneously in a drive circuit integral-type liquid crystal display.
[0013]In this case, since much latch circuitry with a level shift function is needed, the total amount of the current which flows into the 2nd power generation circuit becomes large. On the other hand, it is dramatically difficult to create the power generation circuit which can fully secure current capacity by TFT. It becomes difficult to really form the 2nd power generation circuit on a glass substrate by TFT after all, and it leads to the problem that the area of a peripheral circuit increases.
[0014]Although it is the composition of carrying out a level shift to the signal of the amplitude of VDD-VSS2, about signal in1 of the low-voltage amplitude of VDD-VSS1, and in2 in the latch circuitry concerning the conventional examples 1 and 2, the level shift of power-supply-voltage VDD2 (VDD2>VDD) of the 3rd power supply may be performed further.
[0015]The conventional example is shown in drawing 12 and drawing 13. Drawing 12 is the conventional example 3 corresponding to drawing 10, and drawing 13 is the conventional example 4 corresponding to drawing 11. The latch circuitry concerning the conventional example 3 has composition provided with the 2nd level shift circuit 111 connected to the latter part of the level shift circuit 104 between the power source line 110 of power-supply-voltage VDD2 higher than the power supply voltage VDD, and the power source line 109 of power-supply-voltage VSS2. On the other hand, the latch circuitry concerning the conventional example 4 has the composition that CMOS latch cell 203 itself was connected between the power source line 208 of power-supply-voltage VDD2 higher than the power supply voltage VDD, and the power source line 205 of power-supply-voltage VSS2.

[0016]Also in the case of the latch circuitry concerning the latch circuitry concerning this conventional example 3, and the conventional example 4, it will have the same problem as the case of the latch circuitry concerning the latch circuitry concerning the conventional example 1 which carried out point **, and the conventional example 2.
[0017]in light of the above-mentioned problems, this invention comes out. There is the purpose in providing the liquid crystal display which carries the latch circuitry and this in which small-area-izing is possible while being able to control the flowing current.

[0018]
[Means for Solving the Problem]Latch circuitry by this invention makes a CMOS latch cell basic constitution, and is established at least in one side by the side of a positive supply of this CMOS latch cell, and a negative supply, It has composition provided with the 1st and 2nd switch that chooses the 1st and 2nd power supply from which power supply voltage differs, respectively, and a control means which carries out switching control of the 1st and 2nd switch according to each period of latch operation of a CMOS latch cell, and output operation.
[0019]A liquid crystal display by this invention is a drive circuit integral-type liquid crystal display which really forms a drive circuit including a scanning system on the same substrate as a picture element part, and constitutes using latch circuitry of the one above-mentioned composition [at a component circuit of a scanning system].
[0020]In a liquid crystal display which carries latch circuitry of the above-mentioned composition, and this, in a period of latch operation, latch operation is performed on a basis of the 1st power supply, and the sampling latch of the input signal is carried out to a CMOS latch cell by making the 1st switch one (close). Next, in a period of output operation, level conversion (level shift) and output operation are performed on a basis of the 2nd power supply to which power supply voltage differs from the 1st power supply by that the 2nd switch makes it one. As a result, a signal of amplitude decided by the 1st power supply voltage is drawn as a signal of amplitude decided by the 2nd power supply voltage.
[0021]
[Embodiment of the Invention]Hereafter, it explains in detail, referring to drawings for an embodiment of the invention.
[0022]Drawing 1 is a circuit diagram showing an example of the composition of the latch circuitry concerning a 1st embodiment of this invention. The N-channel metal oxide semiconductor to which each gate and drain were connected to the latch circuitry concerning this 1st embodiment in common, respectively. (It is only hereafter described as NMOS) CMOS inverter 11 which consists of transistor Qn11 and P channel MOS (it is only hereafter described as PMOS) transistor Qp11, CMOS inverter 12 with which each gate and drain consist of NMOS transistorQn12 and PMOS transistorQp12 which were connected in common, respectively makes basic constitution CMOS latch cell 10 which it comes to connect in parallel mutually.
[0023]In this CMOS latch cell 10, the common gate node of the input edge of CMOS inverter 11, i.e., MOS transistorQn11, and Qp11, The drain common node of the outgoing end of CMOS inverter 12, i.e., MOS transistorQn12, and Qp12 is connected, Furthermore, the drain common node of the common gate node of the input edge of CMOS inverter 12, i.e., MOS transistorQn12, and Qp12 and the outgoing end of CMOS inverter 11, i.e., MOS transistorQn11, and Qp11 is connected.
[0024]The switch 15 is connected between the input edge of CMOS inverter 11, and the 1st circuit input terminal 13, and the switch 16 is connected between the input edge of CMOS inverter 12, and the 2nd circuit input terminal 14. The outgoing end of CMOS inverter 12 is connected to the 1st circuit output terminal 17, and the outgoing end of CMOS inverter 11 is connected to the 2nd circuit output terminal 18, respectively. And two output signal out1 of reverse polarity (opposite phase) and out2 are mutually drawn through these circuit output terminals 17 and 18.
[0025]As for the positive supply side of this CMOS latch cell 10, direct continuation of the node A is carried out to the power source line 19 of the positive power supply voltage VDD. As for the negative supply side, the node B is connected to the power source line 23 of power-supply-voltage (negative supply voltage) VSS2 lower than

power-supply-voltage VSS1 via the switch 21 while being connected to the power source line 22 of negative supply side voltage (for example, grand level) VSS1 via the switch 20.
[0026]Switching control of the switch 20 is carried out with the switches 15 and 16 by output enable pulse oe1 inputted into the input terminal 24 from the control circuit which is not illustrated. On the other hand, switching control of the switch 21 is carried out by output enable pulse oe2 inputted into the input terminal 25 from the above-mentioned control circuit.
[0027]In the latch circuitry concerning a 1st embodiment of the above-mentioned composition, signal in1 with the amplitude of VDD-VSS1 shall be inputted into the 1st circuit input terminal 13, and inversion signal in2 of input signal in1 shall be inputted into the 2nd circuit input terminal 14. Here, the circuit operation of the latch circuitry concerning a 1st embodiment is explained using the timing chart of drawing 2.
[0028]First, if output enable pulse oe1 of active"H" is inputted into the input terminal 24, this will be answered, the switches 15 and 16 will be in an one (close) state, input signal in1 and in2 will be sampled, and it will transmit to CMOS latch cell 10. Thereby, input signal in1 and in2 are once latched to CMOS latch cell 10 with the amplitude of VDD-VSS1.
[0029]While the switch 20 answers output enable pulse oe1 and is in an ON state in the period of this latch operation, Since output enable pulse oe2 is in the reverse polarity ("L" level) of output enable pulse oe1 and the switch 21 is in an OFF (open) state, the negative supply side of CMOS latch cell 10 will be connected to the power source line 22 of power-supply-voltage VSS1.
[0030]Next, while output enable pulse oe1 changes on the "L" level, when output enable pulse oe2 changes on "H" level, it shifts to the period of output operation. In this period, since the switch 20 will be in an OFF state and the switch 21 will be in an ON state, the negative supply side of CMOS latch cell 10 will be connected to the power source line 23 of power-supply-voltage VSS2.
[0031]By this, in CMOS latch cell 10, the signal latched with the amplitude of VDD-VSS1 till then will have the amplitude of VDD-VSS2. And the signal of the amplitude of this VDD-VSS2 will be outputted as signal out1 and out2. As a result, the sampling latch of signal in1 with the amplitude of VDD-VSS1 and in2 can be carried out, and level conversion (level shift) can be carried out to signal out1 with the amplitude of VDD-VSS2, and out2.
[0032]As mentioned above, in the latch circuitry concerning a 1st embodiment. In the latch circuitry which makes CMOS latch cell 10 basic constitution, and has a level shift function, The two switches 20 and 21 which choose VSS1 power supply and VSS2 power supply as the negative supply side of CMOS latch cell 10 are formed, By having been made to carry out switching control of these switches 20 and 21 according to each period of the latch operation of CMOS latch cell 10, and output operation, In the period of latch operation, CMOS latch cell 10 will operate with VSS1 power supply, and will operate with VSS2 power supply in the period of output operation.
[0033]In order for many of charging current for being able to control by this the current which flows into the power supply of VSS1/VSS2, and charging especially output load to flow toward VSS1 power supply from a VDD power supply, there is dramatically little current which flows into VSS2 power supply. And while latch operation and level shift operation are realizable with the small number of circuit elements, Since it is not necessary to rewrite the latch for the signals of high-tension amplitude compulsorily by the signal of low-voltage amplitude, and the size of the signal buffer of the preceding paragraph is small and ends, latch circuitry with a level shift function of small-area-izing can be realized.
[0034]Another example of timing is shown in drawing 3. In the example of timing of drawing 3, falling of output enable pulse oe2 a little rather than the standup of output enable pulse oe1 Early, The standup of output enable pulse oe2 is late a little rather than falling of output enable pulse oe1. By using such timing relationship, the current which flows into VSS2 power supply can be reduced certainly.
[0035]Drawing 4 is a circuit diagram showing the example of the latch circuitry concerning a 1st embodiment, and attaches and shows identical codes among the figure to drawing 1 and an equivalent portion. In the latch circuitry concerning this example, as the switches 15, 16, 20, and 21 of drawing 1, NMOS transistorQn13, Qn14, Qn15, and Qn16 are used, It has the composition of having impressed output enable pulse oe1 to each gate of transistor Qn13, Qn14, and Qn15, and having made it impress output enable pulse oe2 to the gate of transistor Qn16,

respectively.
[0036]Thus, when the switches 15, 16, 20, and 21 are realized with a transistor, operation of the circuit is also the same as the case of the circuit of drawing 1. It is the same as drawing 2 and drawing 3 also about the example of timing. Although NMOS has realized the switches 15, 16, 20, and 21 in this example, when output enable pulse oe1 and oe2 are active"L", it is clear the polarity's to become reverse.
[0037]Drawing 5 is a circuit diagram showing an example of the composition of the latch circuitry concerning a 2nd embodiment of this invention. CMOS inverter 31 with which the latch circuitry concerning this 2nd embodiment consists of NMOS transistorQn31 and PMOS transistorQp31 to which each gate and drain were connected in common, respectively, CMOS inverter 32 with which each gate and drain consist of NMOS transistorQn32 and PMOS transistorQp32 which were connected in common, respectively makes basic constitution CMOS latch cell 30 which it comes to connect in parallel mutually.
[0038]In this CMOS latch cell 30, the common gate node of the input edge of CMOS inverter 31, i.e., MOS transistorQn31, and Qp31, The drain common node of the outgoing end of CMOS inverter 32, i.e., MOS transistorQn32, and Qp32 is connected, Furthermore, the drain common node of the common gate node of the input edge of CMOS inverter 32, i.e., MOS transistorQn32, and Qp32 and the outgoing end of CMOS inverter 31, i.e., MOS transistorQn31, and Qp31 is connected.
[0039]The switch 35 is connected between the input edge of CMOS inverter 31, and the 1st circuit input terminal 33, and the switch 36 is connected between the input edge of CMOS inverter 32, and the 2nd circuit input terminal 34. The outgoing end of CMOS inverter 32 is connected to the 1st circuit output terminal 37, and the outgoing end of CMOS inverter 31 is connected to the 2nd circuit output terminal 38, respectively. And two output signal out1 of reverse polarity (opposite phase) and out2 are mutually drawn through these circuit output terminals 37 and 38.
[0040]As for the positive supply side of this CMOS latch cell 30, the node A is connected to the power source line 42 of power-supply-voltage VDD2 higher than power-supply-voltage VDD1 via the switch 40 while being connected to the power source line 41 of positive-supply-voltage VDD1 via the switch 39. As for the negative supply side, direct continuation of the node B is carried out to the power source line 43 of negative supply side voltage (for example, grand level) VSS.
[0041]Switching control of the switch 39 is carried out with the switches 35 and 36 by output enable pulse oe1 inputted into the input terminal 44 from the control circuit which is not illustrated. On the other hand, switching control of the switch 40 is carried out by output enable pulse oe2 inputted into the input terminal 45 from the above-mentioned control circuit.
[0042]In the latch circuitry concerning a 2nd embodiment of the above-mentioned composition, signal in1 with the amplitude of VDD1-VSS shall be inputted into the 1st circuit input terminal 33, and inversion signal in2 of input signal in1 shall be inputted into the 2nd circuit input terminal 34. The pulse in the timing relationship of drawing 2 or drawing 3 as well as as output enable pulse oe1 and oe2 the case of the latch circuitry concerning a 1st embodiment is inputted.
[0043]Thereby, in the latch circuitry concerning a 2nd embodiment, the fundamentally same operation as the latch circuitry concerning a 1st embodiment is performed. That is, in the period of latch operation with active output enable pulse oe1, it operates under VDD1 power supply and signal in1 with the amplitude of VDD1-VSS and in2 are once latched with the same amplitude as CMOS latch cell 30 through the switches 35 and 36.
[0044]Next, output enable pulse oe2 in the period of active output operation. Since the power supply by the side of right [of CMOS latch cell 30] switches from VDD1 power supply to VDD2 power supply, the level shift of the signal with the amplitude of VDD1-VSS will be carried out to the signal of the amplitude of VDD2-VSS, and this will be drawn as output signal out1 and out2.
[0045]As mentioned above, in the latch circuitry concerning a 2nd embodiment. By forming the two switches 39 and 40 for power supply selection, and carrying out switching control of these switches 39 and 40 to the positive supply side of CMOS latch cell 30 according to each period of the latch operation of CMOS latch cell 30, and output operation, In order to operate with VDD1 power supply in the period of latch operation and to operate with

VDD2 power supply in the period of output operation, While being able to control the current which flows into the power supply of VDD1/VDD2 as well as the case of a 1st embodiment and being able to constitute from a small number of circuit elements moreover, Since it is not necessary to rewrite the latch for the signals of high-tension amplitude compulsorily by the signal of low-voltage amplitude, and the size of the signal buffer of the preceding paragraph is small and ends, small area-ization is attained.

[0046]Drawing 6 is a circuit diagram showing an example of the composition of the latch circuitry concerning a 3rd embodiment of this invention. CMOS inverter 51 with which the latch circuitry concerning this 3rd embodiment consists of NMOS transistorQn51 and PMOS transistorQp51 to which each gate and drain were connected in common, respectively, CMOS inverter 52 with which each gate and drain consist of NMOS transistorQn52 and PMOS transistorQp52 which were connected in common, respectively makes basic constitution CMOS latch cell 50 which it comes to connect in parallel mutually.

[0047]In this CMOS latch cell 50, the common gate node of the input edge of CMOS inverter 51, i.e., MOS transistorQn51, and Qp51, The drain common node of the outgoing end of CMOS inverter 52, i.e., MOS transistorQn52, and Qp52 is connected, Furthermore, the drain common node of the common gate node of the input edge of CMOS inverter 52, i.e., MOS transistorQn52, and Qp52 and the outgoing end of CMOS inverter 51, i.e., MOS transistorQn51, and Qp51 is connected.

[0048]The switch 55 is connected between the input edge of CMOS inverter 51, and the 1st circuit input terminal 53, and the switch 56 is connected between the input edge of CMOS inverter 52, and the 2nd circuit input terminal 54. The outgoing end of CMOS inverter 52 is connected to the 1st circuit output terminal 57, and the outgoing end of CMOS inverter 51 is connected to the 2nd circuit output terminal 58, respectively. And two output signal out1 of reverse polarity (opposite phase) and out2 are mutually drawn through these circuit output terminals 57 and 58.

[0049]As for the positive supply side of this CMOS latch cell 50, the node A is connected to the power source line 62 of power-supply-voltage VDD2 higher than power-supply-voltage VDD1 via the switch 60 while being connected to the power source line 61 of positive-supply-voltage VDD1 via the switch 59. As for the negative supply side, the node B is connected to the power source line 66 of power-supply-voltage (negative supply voltage) VSS2 lower than power-supply-voltage VSS1 via the switch 64 while being connected to the power source line 65 of negative supply side voltage (for example, grand level) VSS1 via the switch 63.

[0050]Switching control of the switches 59 and 63 is carried out with the switches 55 and 56 by output enable pulse oe1 inputted into the input terminal 67 from the control circuit which is not illustrated. On the other hand, switching control of the switches 60 and 64 is carried out by output enable pulse oe2 inputted into the input terminal 68 from the above-mentioned control circuit.

[0051]In the latch circuitry concerning a 3rd embodiment of the above-mentioned composition, signal in1 with the amplitude of VDD1-VSS shall be inputted into the 1st circuit input terminal 53, and inversion signal in2 of input signal in1 shall be inputted into the 2nd circuit input terminal 54. The pulse in the timing relationship of drawing 2 or drawing 3 as well as as output enable pulse oe1 and oe2 the case of the latch circuitry concerning a 1st and 2nd embodiment is inputted.

[0052]Thereby, in the latch circuitry concerning a 3rd embodiment, the fundamentally same operation as the latch circuitry concerning a 1st and 2nd embodiment is performed. Namely, output enable pulse oe1 in the period of active latch operation. It operates under each power supply of VDD1 and VSS1, and signal in1 with the amplitude of VDD1-VSS1 and in2 are once latched with the same amplitude as CMOS latch cell 50 through the switches 55 and 56.

[0053]Next, output enable pulse oe2 in the period of active output operation. While the power supply by the side of right [of CMOS latch cell 50] switches from VDD1 power supply to VDD2 power supply, Since the power supply of a negative side switches from VSS1 power supply to VSS2 power supply, the level shift of the signal with the amplitude of VDD1-VSS1 will be carried out to the signal of the amplitude of VDD2-VSS2, and this will be drawn as output signal out1 and out2.

[0054]As mentioned above, in the latch circuitry concerning a 3rd embodiment. The two switches 59 and 60 and

the switches 63 and 64 are formed in the positive supply [of CMOS latch cell 50], and negative supply side as an object for power supply selection, respectively, By carrying out switching control of these switches 59 and 60 and the switches 63 and 64 according to each period of the latch operation of CMOS latch cell 50, and output operation, In order to operate with each power supply of VDD1 and VSS1 in the period of latch operation and to operate with each power supply of VDD2 and VSS2 in the period of output operation, While being able to control the current which flows into each power supply as well as the case of a 1st and 2nd embodiment and being able to constitute from a small number of circuit elements moreover, Since it is not necessary to rewrite the latch for the signals of high-tension amplitude compulsorily by the signal of low-voltage amplitude, and the size of the signal buffer of the preceding paragraph is small and ends, small area-ization is attained.

[0055]The switches 35, 36, 39, and 40 in drawing 5 and the switches 55, 56, 59, 60, 63, and 64 in drawing 6 are realizable with a transistor about the latch circuitry concerning a 2nd and 3rd embodiment of the above as well as the example (see drawing 4) of a 1st embodiment. However, each inversion signal of output enable pulse oe1 and oe2 will be used as a signal with which a PMOS transistor is preferred and switches these in this case as the switches 39 and 40 in drawing 5, and the switches 59 and 60 in drawing 6.

[0056]Although it had composition which derives two output signal out1 which is an inversion signal mutually, and out2 in the latch circuitry concerning a 1st, 2nd, and 3rd embodiment, it may be the composition which derives only one of output signals.

[0057]The latch circuitry with a level shift function concerning a 1st, 2nd, and 3rd embodiment of this invention explained above, For example, on the glass substrate in which poly-Si TFT has been arranged as a switching element of each pixel at two-dimensional matrix form, In the drive circuit integral-type liquid crystal display which a picture element part and really forms a digital interface drive circuit by poly-Si TFT, it is used as the 2nd latch circuitry of the level drive system. An example of the composition of a drive circuit integral-type liquid crystal display is shown in drawing 7.

[0058]In drawing 7, the level drive system 72 is allotted to the valid pixel area 71 upper part where it comes to arrange a pixel at two-dimensional matrix form, and the vertical-drive system 73 is allotted to left-hand side, and it has composition really formed on the glass substrate with the valid pixel area 71 by poly-Si TFT. The level drive system 72 is constituted by the horizontal shift register 721, the sampling & 1st latch circuitry 722, the 2nd latch circuitry 723, and the DA (digital analog) converter 724. The vertical-drive system 73 is constituted by the vertical driver 731 containing a shift register.

[0059]In the level drive system 72, horizontal start pulse HST and the horizontal clock pulse HCK are given to the horizontal shift register 721 as a horizontal transfer pulse. Then, the horizontal shift register 721 performs a horizontal scanning by answering horizontal start pulse HST and outputting a shift pulse one by one from each stage with the cycle of the horizontal clock pulse HCK. The sampling & 1st latch circuitry 722 answers the shift pulse outputted from the horizontal shift register 721, and latches the data which sampled digital data one by one and sampled it further for every column line of the valid pixel area 71.

[0060]The 2nd latch circuitry 723 answers the latch signal which can be given 1H (H is a horizontal scanning period) cycle, and re-latches the latch data corresponding to the column line latched in the sampling & 1st latch circuitry 722 for everyH. DA converter 724 changes into an analog signal the digital data re-latched to the 2nd latch circuitry 723 for every column line, and supplies this analog signal to a corresponding column line.

[0061]In the drive circuit integral-type liquid crystal display of the above-mentioned composition, the latch circuitry with a level shift function concerning a 1st, 2nd, and 3rd embodiment of this invention is used as the 2nd latch circuitry 723. A latch pulse is given to the 2nd latch circuitry 723 via the buffer 74. The drive circuit containing the horizontal scanning system 72 and the vertical-drive system 73 and the 2nd power generation circuit 75 that generates the 2nd power supply VDD2/VSS2 similarly are a picture element part and really formed by poly-Si TFT.

[0062]Thus, by being able to realize with a small area and carrying the latch circuitry with a level shift function of low power consumption as the 2nd latch circuitry 723, A drive circuit and the 2nd power generation circuit 75 including the latch circuitry 723 concerned, such as the level drive system 72 and the vertical-drive system 73,

When creating on the same substrate as the valid pixel area 71, while being able to narrow the adjacent spaces (frame) of the valid pixel area 71 which allots the drive circuit concerned, the drive circuit integral-type liquid crystal display of low power consumption can be realized.

[0063]Below, the example of application to a drive circuit integral-type liquid crystal display is explained. Drawing 8 is a block diagram showing the example at the time of using the latch circuitry (see drawing 1) concerning a 1st embodiment of this invention as the 2nd latch circuitry 723, for example, shows the example in the case of inputting the digital data b0 of a triplet, b1, and b2.

[0064]Sampling latch circuit 722-1,722-2,722-3 is formed every bit of the digital data b0, b1, and b2, and latch circuitry 723-1,723-2,723-3 is further formed in the latter part, respectively so that clearly from drawing 8. Sampling latch circuit 722-1,722-2,722-3, Each bit data of the digital data b0, b1, and b2 are considered as an input, and each input data is sampled according to the sampling pulse outputted from the horizontal shift register 72 (see drawing 7).

[0065]On the other hand, to latch circuitry 723-1,723-2,723-3. While each sampling data are supplied from sampling latch circuit 722-1,722-2,722-3, Output enable pulse oe1 outputted from the buffer 74 based on the latch pulse inputted from the outside and oe2 are inputted as a latch pulse, and it has the composition that VSS2 power supply is further supplied as the 2nd power supply of a negative side from the 2nd power generation circuit 75.

[0066]By this latch circuitry 723-1,723-2,723-3, After answering output enable pulse oe1 and carrying out the sampling latch of each sampling data of sampling latch circuit 722-1,722-2,722-3 of the preceding paragraph, Level conversion to signal amplitude required for the synchronization (formation of line sequential) of data and the DA translation of the next step is performed in the timing of output enable pulse oe2, and it outputs to the column line with which the valid pixel area 71 corresponds through DA converter 724 after an appropriate time.

[0067]With thus, the drive circuit of the level drive system 72 including the 2nd latch circuitry 723 or the vertical-drive system 73. In the drive circuit integral-type liquid crystal display of composition of really forming the 2nd power generation circuit 75 by TFT, Since he is trying to use a power supply properly in each period of latch operation/output operation in the latch circuitry concerned by using the latch circuitry concerning a 1st embodiment of this invention as the 2nd latch circuitry 723, the current which flows into the 2nd power generation circuit 75 can be controlled. Since the 2nd latch circuitry 723 is realizable with a small area by this while built-in(one formation)-ization to the liquid crystal panel of the 2nd power generation circuit 75 becomes easy, narrow picture frame-ization of a liquid crystal panel is attained.

[0068]Drawing 9 is a block diagram showing the modification of drawing 8, and gives identical codes to drawing 8 and an equivalent portion among the figure. In this modification, the switches 76 and 77 are formed as a switch (equivalent to the switches 20 and 21 of drawing 1) by the side of the negative supply of each latch circuitry 723-1,723-2,723-3, and it has composition which shared these switches 76 and 77 between each circuit 723-1,723-2,723-3.

[0069]According to this composition, digital data in the example of a triplet. As opposed to the switch for two pieces and a total of six power supply changes in the switch by the side of a negative supply being required to each of three latch circuitry corresponding to a triplet, when the circuit of drawing 1 is used as it was, Since it will end with two switches to three latch circuitry and four switches for a power supply change can be reduced, the further small area-ization will be attained and, therefore, narrow picture frame-ization can be realized from that of a liquid crystal panel.

[0070]Although it presupposed that the latch circuitry concerning a 1st embodiment is used as the 2nd latch circuitry 723 in this example, it is also possible to use the latch circuitry concerning a 2nd and 3rd embodiment, and the same operation effect can be obtained.

[0071]Although this example explained taking the case of the case where the latch circuitry with a level shift function concerning this invention is applied to the 2nd latch circuitry 723 of the level drive system 72 in a drive circuit integral-type liquid crystal display, It is applicable to a circuit system at large [using not the thing restricted to this but TFT formed on the silicon substrate].

[0072]
[Effect of the Invention]As explained above, according to this invention, the power supply of the right side of a CMOS latch cell and a negative side at least to one side. Since the current which flows into each power supply by preparing two switches for choosing a power supply, and having been made to carry out switching control of these switches according to each period of latch operation/output operation can be controlled and it can moreover constitute from a small number of circuit elements, it can realize with a small area.

[Translation done.]

CLAIMS

[Claim(s)]
[Claim 1]Latch circuitry comprising:
The 1st and 2nd switch that chooses the 1st and 2nd power supply from which makes a CMOS latch cell basic constitution, it is provided at least in one side by the side of a positive supply of said CMOS latch cell, and a negative supply, and power supply voltage differs, respectively.
A control means which carries out switching control of said 1st and 2nd switch according to each period of latch operation of said CMOS latch cell, and output operation.

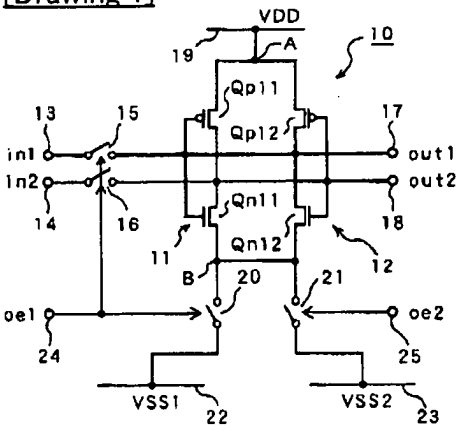
[Claim 2]The latch circuitry according to claim 1, wherein said 1st and 2nd switch is realized with a transistor.
[Claim 3]Latch circuitry, wherein two or more latch circuitry according to claim 1 is arranged and said 1st and 2nd switch is shared to two or more of these latch circuitry.
[Claim 4]The latch circuitry according to claim 1 currently creating using a thin film transistor formed on a glass substrate.
[Claim 5]The latch circuitry according to claim 1 currently creating using a thin film transistor formed on a silicon substrate.
[Claim 6]A liquid crystal display which really forms a drive circuit characterized by comprising the following including a scanning system on the same substrate as a picture element part.
The 1st and 2nd switch that chooses the 1st and 2nd power supply from which makes a CMOS latch cell basic constitution, it is provided at least in one side by the side of a positive supply of said CMOS latch cell, and a negative supply, and power supply voltage differs said scanning system, respectively.
A control means which carries out switching control of said 1st and 2nd switch according to each period of latch operation of said CMOS latch cell, and output operation.

[Claim 7]The liquid crystal display according to claim 6, wherein said 1st and 2nd switch is realized with a transistor.
[Claim 8]The liquid crystal display according to claim 6, wherein two or more said latch circuitry is arranged corresponding to the number of bits of digital data and said 1st and 2nd switch is shared to two or more of these latch circuitry.

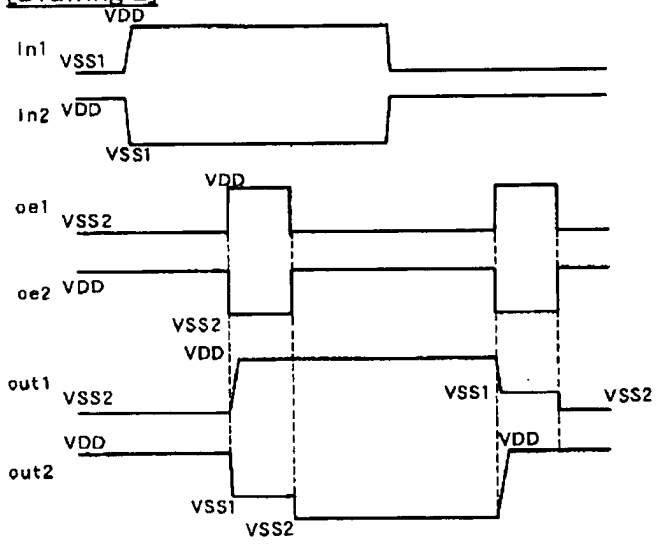
[Translation done.]

DRAWINGS

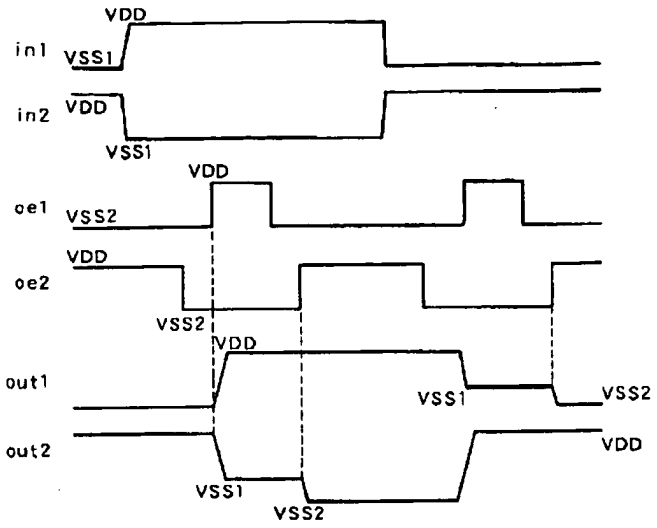
[Drawing 1]



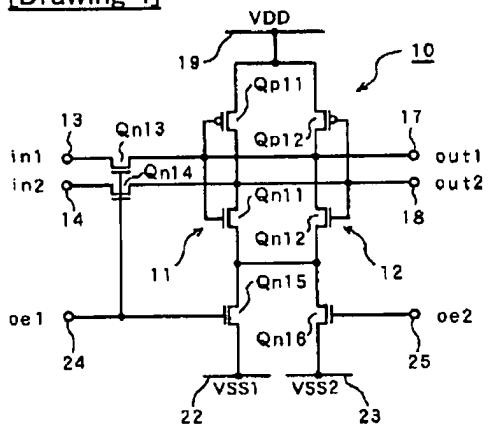
[Drawing 2]



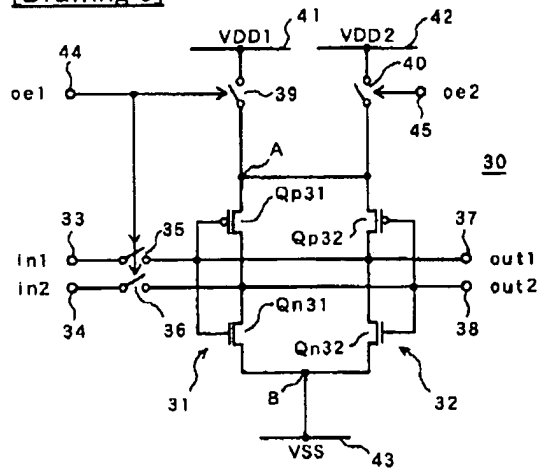
[Drawing 3]



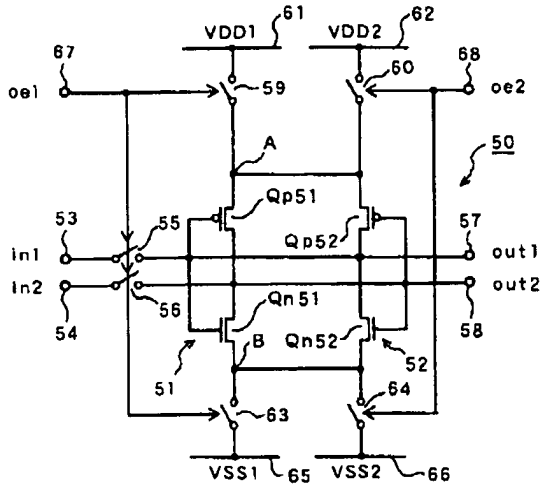
[Drawing 4]



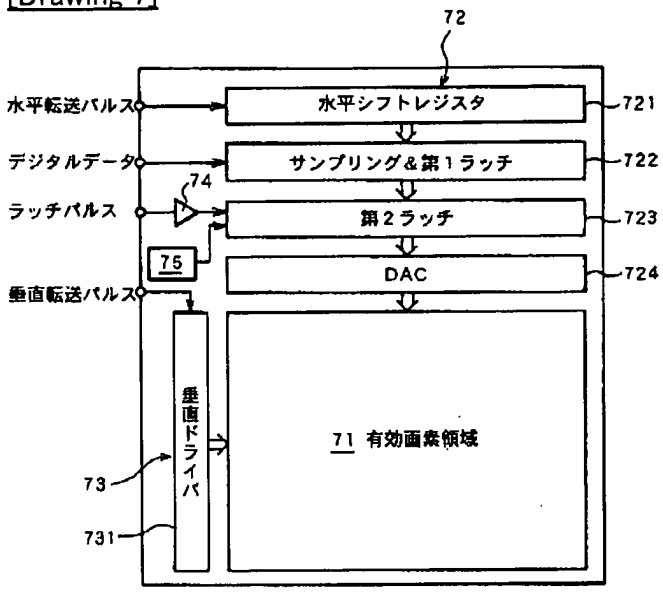
[Drawing 5]



[Drawing 6]

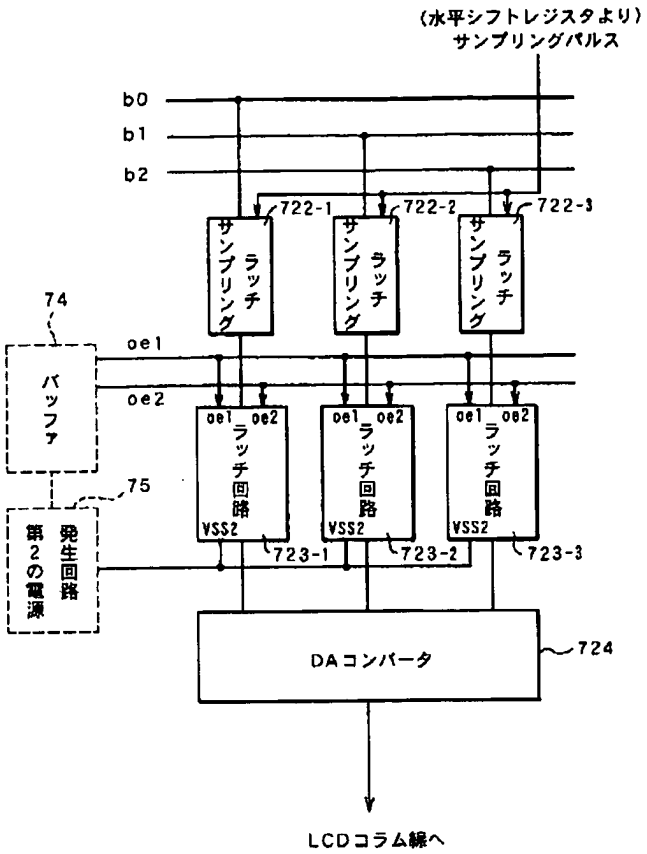


[Drawing 7]

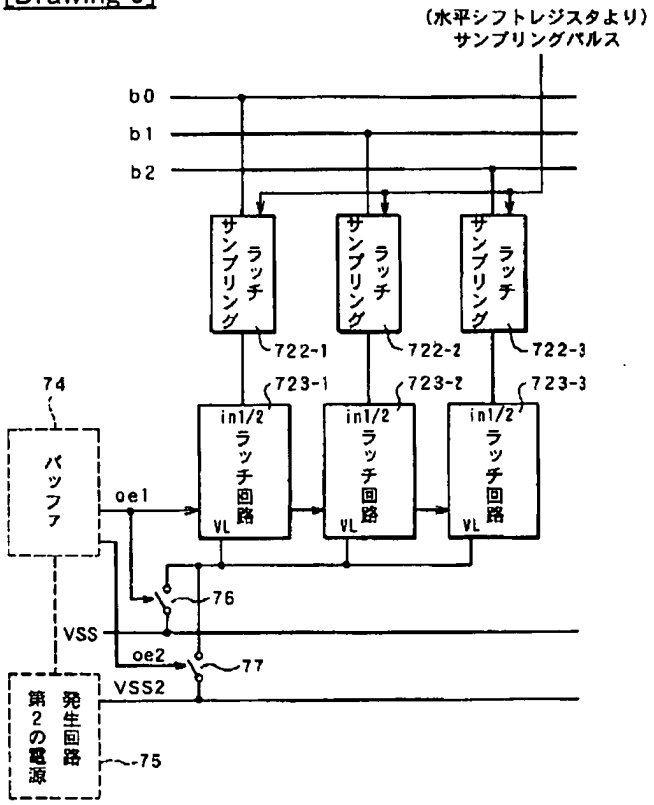


75 第２の電源発生回路

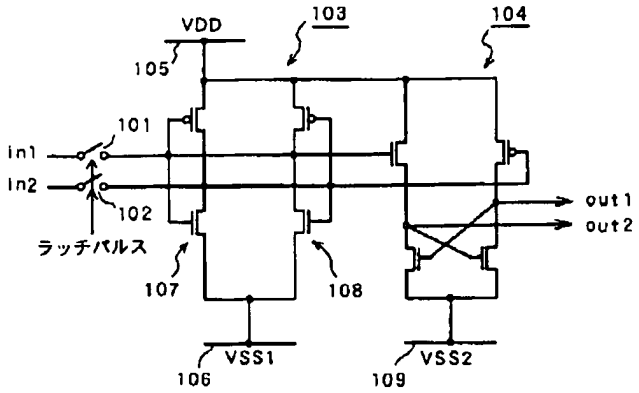
[Drawing 8]



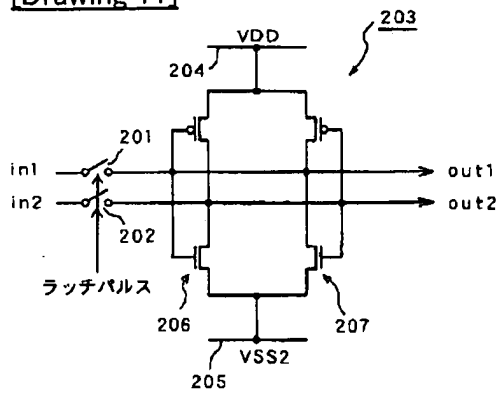
[Drawing 9]



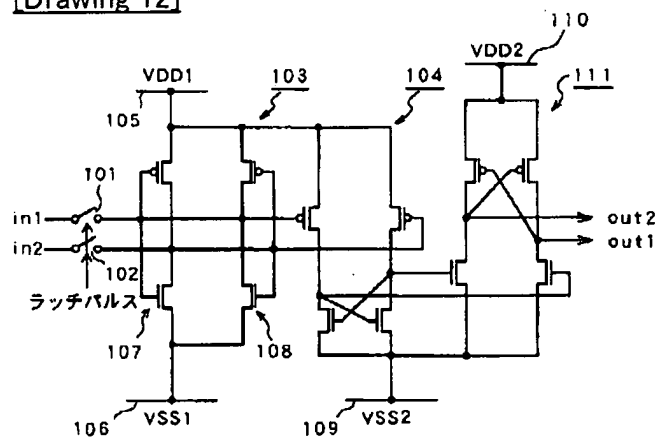
[Drawing 10]



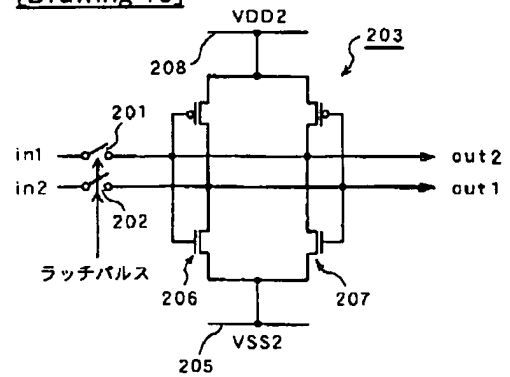
[Drawing 11]



[Drawing 12]



[Drawing 13]



[Translation done.]